## REMARKS

The Examiner is thanked for the thorough review and consideration of the present application. The final Office Action dated March 22, 2004 has been received and its contents carefully reviewed.

By this Response, claims 12, 16 and 19-21 have been amended, and claim 23 has been cancelled without prejudice or disclaimer of the subject matter recited therein. No new matter has been added. Claims 1-22 and 24-25 are pending in the application, with claims 1-11 being withdrawn from consideration. Reconsideration and withdrawal of the rejection in view of the above amendments and the following remarks are requested.

In the Office Action, claims 12-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Related Art in view of U.S. Patent No. 5,990,9887, issued to Tanaka. Applicant respectfully traverses the rejection because neither the Related Art nor Tanaka, analyzed alone or in any combination, teaches nor suggests the combined features recited in the claims of the present application. For example, neither the Related Art nor Tanaka teaches or suggests a method of forming an array substrate for an in-plane switching liquid crystal display device that includes, among other features, "simultaneously patterning an active layer and an ohmic contact layer on the gate insulation layer using a second mask," as recited in independent claim 12 of the present application.

The Office Action concedes that Related Art fails to teach all the features of the present application and relies upon the teachings of Tanaka to remedy the deficiencies of the Related Art. Applicant respectfully submits Tanaka fails to remedy the deficiencies of the Related Art such that one of ordinary skill in the art would be motivated by the teachings of Tanaka to modify the Related Art to obtain a method of forming an array substrate for an in-plane switching liquid crystal display device that includes the combined features recited in claim 12. Specifically, in Tanaka, "the insulating substrate 1 is processed with plasma (pressure of 150 Pa, PH3/Ar mixed gas (Ph3: 5000 ppm), flow of 1000 sccm, RF power of 50 W, and discharging time of 60 sec) to form an n-type semiconductor layer 7 selectively on only the low-resistance metal film. On the resulting assembly, there are also formed a semiconductor film 4..." (see, col. 4, lines 51-56, emphasis added). As such, the n-type semiconductor layer 7 and the semiconductor film 4 are formed using separate photolithographic processes. Whereas, claim 12 of the present application requires "simultaneously patterning an active layer and an ohmic

contact layer on the gate insulation layer using a second mask." Accordingly, no combination of the Related Art and Tanaka teaches the combined features recited in independent claim 12. Thus, claim 12 and its dependent claims 13-22 and 24-25 are allowable over the Related Art and Tanaka. Reconsideration and withdrawal of the rejection are requested.

Additionally, Applicant notes on page 4 of the Office Action, a broad statement of "a very well known practice in the art" regarding the limitation of "simultaneously thermal-treating the alignment layer, the source electrode and the drain electrode," as recited in independent claim 12. In particular, the Office Action states that "it would have at least been obvious to one of ordinary skill in the art at the time the invention was made to simultaneously thermal treating the alignment layer, the source electrode and the drain electrode to reduce manufacturing steps and thus cost." As stated in paragraph [0028] of Applicant's specification, "[t]he heat treatment process of curing the alignment layer is generally executed under the condition of annealing the thin film transistor. Namely, the heat treatment process has the same process condition as the annealing process. However, since these processes are carried out at different times in the array process and the cell process, there are problems of increasing the production cost and time." The claims of the present application provide a solution to these problems that is not taught in the references of record. It appears that through hindsight, the Examiner is concluding that the recited solution to the problem is obvious. Further, it appears that the Examiner is taking Official Notice that "it is very well known practice in the art to reduce manufacturing steps and thus cost." Applicants therefore request that the Examiner provide a reference showing such a teaching. This request is being made according to MPEP §2144.03. Absent such teaching in the art and in view of the failure of the art of record to teach the recited features of claim 12, Applicant respectfully traverses the Office Action's assertion and request the Examiner to provide documentary support for the assertion in any next office action if the rejection is maintained.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue. If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

By Valerie Hayes

Valerie Hayes
Registration No.: 53,005
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorney for Applicant